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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,552	08/02/2003	Marcos Karnezos	CPAC 1017-5	2572

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,552	KARNEZOS, MARCOS	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 17 and 19 - 36* is/are pending in the application.

4a) Of the above claim(s) *20 - 34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 17, 19, 35 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/4/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 4, 2005 has been entered. An action on the RCE follows.

Response to Amendment

2. Applicant's amendment filed on October 4, 2005 has been received and entered in the case.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Maeda (JP 2001-223,326).

Regarding claim 1, Maeda discloses in e.g., Fig. 8 and Fig. 2 a multi-package module (12) comprising

- stacked first (1 and 3; abstract, lines 8 and 9) and second packages (2 and 4; abstract, lines 8 – 10),
- each said package including a die (1 and 2) attached to a passive substrate (3 and 4),
- wherein the first (3) and second (4) substrates are interconnected by wire bonding (9; abstract, line 12), and wherein the first package (1 and 3) comprises a flip-chip ball grid array package having a flip-chip (1) in a die-up configuration (see Fig. 8).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 – 5, 11, 12, 17, 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halahan (U. S. Pat. No. 6,787,916) in view of Ichinose et al. (U. S. Pat. No. 6,611,063).

Regarding claim 1, Halahan discloses in e.g., Fig. 1 a multi-package module comprising

- stacked first (166 and 178; column 3, lines 31 and 56) and second packages (108, 104.1 and 104.2; column 2, lines 22 – 23),
- each said package including a die (178, 104.1 and 104.2) attached to a passive substrate (166 and 108),

- wherein the first (166) and second (108) substrates are interconnected by wire bonding (176; column 3, line 51), and
- wherein the first package (166 and 178) comprises a ball grid array package (see e.g., Fig. 1).

However, Halahan does not disclose the first package comprising a flip-chip in a die-up configuration. Ichinose et al. teaches in e.g., Fig. 13 a flip-chip (54C; column 7, lines 66 – 67) in a die-up configuration in a package (see Fig. 13). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to add the die of Ichinose et al. at the bottom of the first substrate, opposing the chip 178 of Halahan as taught by Ichinose et al. to increase the performance of the package without increasing the overall thickness of the semiconductor package (abstract, lines 8 – 9).

Regarding claim 2, Halahan discloses in e.g., Fig. 1 the second package (108, 104.1 and 104.2) being a wire bonded (158) land grid array package (see Fig. 1).

Regarding claim 3, Halahan discloses in e.g., Fig. 1 the die (104.1 and 104.2) and wire bonds (158) in the second package being fully encapsulated with a molding material (the encapsulant; column 7, lines 37 – 39).

Regarding claim 4, Halahan discloses in e.g., Fig. 1 the second package (108, 104.1 and 104.2) being peripherally encapsulated (the encapsulant; column 7, lines 37 – 39) to an extent sufficient to cover the wire bonds (158) between the die (104.1 and 104.2) and the substrate (108).

Regarding claim 5, since Halahan discloses in e.g., Fig. 1 the second package substrate (108) including a single metal layer (150; column 2, lines 53 – 55), the element (150) on the second package substrate (108) reads as a single-metal layer substrate.

Regarding claim 11, Halahan discloses in e.g., Fig. 1 the second package (108, 104.1 and 104.2) being a stacked die package (see Fig. 1).

Regarding claim 12, Halahan discloses in e.g., Fig. 1 adjacent stacked die (104.1 and 104.2) in the stacked die package being separated by spacers (since the adhesive layers between the dice, which could be more than two, separate the dice, the adhesive layers read as spacers).

Regarding claim 17, Halahan discloses in e.g., Fig. 1 at least one of the first and the second package being a stacked-die package (see Fig. 1).

Regarding claims 35 and 36, these claims merely recite the intended use or the environment in which the multi-package module of claim 1 is intended to be used. Since the claims fail to define any additional structure, Halahan anticipates these claims as well.

7. Claims 6 – 10, 13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa et al. in view of Kakimoto et al. (U. S. Pat. No. 6,333,552).

Regarding claims 6, 8, 10 and 13, while Halahan discloses in e.g., Fig. 1 the second package being stacked over the first package (claim 13) and the use of a chip in a flip chip package, Halahan does not appear to provide a specific type of the die to be an RF die (claim 8) and an electrical shield (claims 6, 10 and 13) in the package. Kakimoto et al. teaches in e.g., Fig. 6 and column 1, line 56 – column 2, line 34 an electrical shield (57) and an RF die (30) in a flip chip package (the package in Fig. 7). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to apply the RF die as the specific type of the chip and the electrical shield in the structure

of Halahan as taught by Kakimoto et al. to shield electromagnetic waves (column 1, lines 64 – 65).

Regarding claim 7, Halahan and Kakimoto et al. disclose the electrical shield (57) being a metal cap (column 1, lines 64 and 65). Inherently, every metal cap (57) dissipates heat from a chip. Thus, Halahan and Kakimoto et al. disclose the electrical shield (57) being configured to serve as a heat spreader.

Regarding claim 9, since Halahan and Kakimoto et al. disclose the electrical shield and the RF chip, Halahan and Kakimoto et al. disclose the following limitation "the flip chip package includes an RF die, and the shield serves to limit electromagnetic interference between the RF die and other die in the multi-package module."

Regarding claim 19, since Halahan and Kakimoto et al. disclose a metal cap (57; column 1, lines 64 and 65). Inherently, every metal cap has a function of shielding any external heats from a chip. Thus, Halahan and Kakimoto et al. disclose a heat shield.

8. Claims 14 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halahan in view of Lin (U. S. Pat. No. 5,436,203).

Regarding claim 14, while Halahan discloses in Fig. 1 the use of the first package substrate, Halahan does not appear to provide an embedded ground plane in the first package substrate. Lin teaches in e.g., Fig. 1 and column 6, lines 18 – 20 an embedded ground plane (22) in a package substrate (12). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to apply the embedded ground plane in the first package substrate of Halahan as taught by Lin to establish a

shield surrounding semiconductor die which protects against either external or internal EMI (column 6, lines 18 – 22).

Regarding claim 15, since Halahan and Lin disclose the ground plane (22) being configured to serve for heat dissipation (column 6, lines 61 – 63 of Lin).

Regarding claim 16, since Halahan and Lin disclose the ground plane (22) being configured to serve as an electrical shield (column 6, lines 18 – 22 of Lin).

Response to Arguments

9. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Maeda et al., Mori, Takeda, Hoffman et al., McMahon, Liao et al., Rostoker, Ichikawa and Uchida et al. disclose a stacked semiconductor package.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Thursday, December 01, 2005

SPE Kenneth Parker
TC2800